Fermi National Accelerator Laboratory

Computing Division
Electronic Systems Engineering Department

ESECon Description

--PRELIMINARY--

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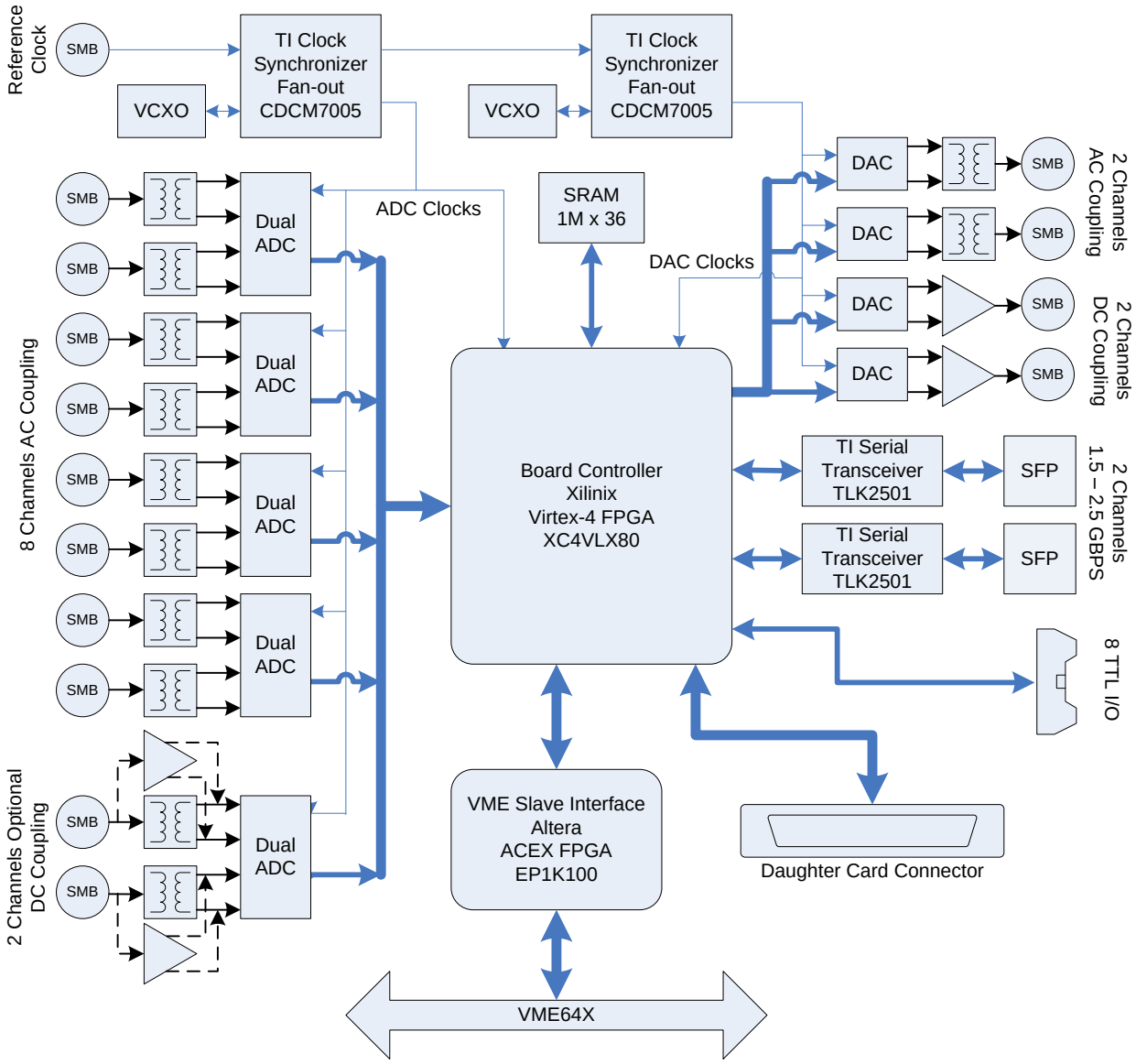
GENERAL INFORMATION

The ESECon is a 10 ADC and 4 DAC channel VME64X module designed for use as an LLRF controller in systems such as the A0 photo injector, CC2, HTS, and the NML cryomodules. The ESECon board was designed to be functionally compatible with DESY's Simcon3.1 controller. Major goals were to minimize the noise at all levels and to lower the power consumption of the ADCs.

FEATURES

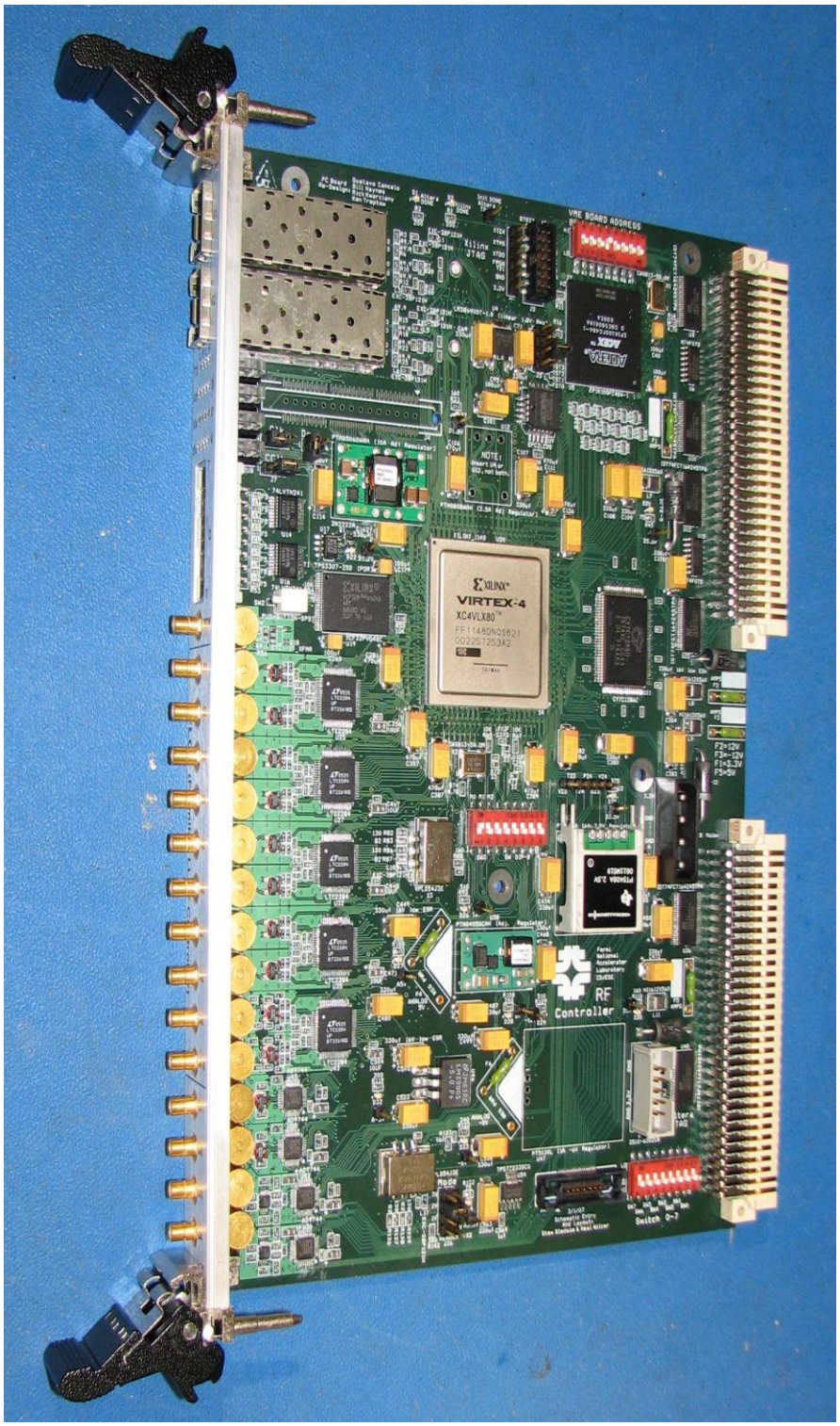
- 10, 14-bit ADC channels using Linear Technologies LTC2284 Dual 105Msps, 540mW ADCs.
- 4, 14-bit DAC channels using Analog Devices AD9744 210Msps, 135mW DACs
- External 0-200MHz reference input.
- 8 TTL I/O signals that are controllable in groups of 4.
- 2 SFP 1.5 to 2.5Gbps serial transceiver links using Texas Instruments TLK2501 transceiver ICs.
- Xilinix XC4VLX80 Virtex-4 FPGA that is used to control all functions except VME.
- 2 Texas Instruments CDCM7005 PLL clock synchronizer and jitter cleaner ICs for onboard clock generation.
- 1M x 36bit Sync SRAM.
- VME64X Slave interface using Altera EP1K100 ACEX FPGA.
- 114 pin daughter card connector.
- Single width 6U VME64X module.
- 8 front panel LED indicators defined by Xilinx FPGA firmware.
- 4 front panel LED indicators defined by Altera FPGA firmware.
- 4 dedicated front panel LED indicators connected to the SFP link status.
- Quiet power supplies with a mixture of switched and linear.

Block Diagram



ESECon Block Diagram

Picture



HARDWARE DETAILS AND PERFORMANCE MEASUREMENTS

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PLL Information

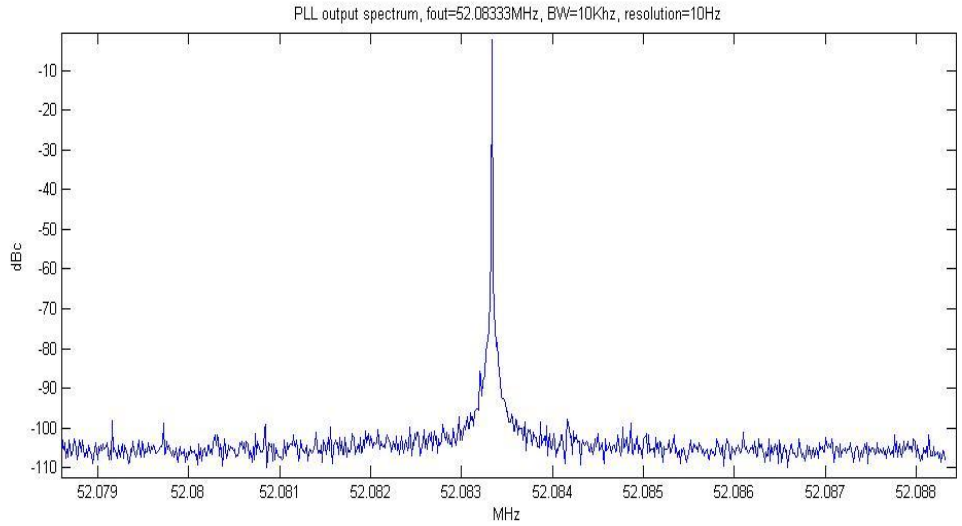
The ESECon uses two TI CDCM7005 High Performance Clock Synchronizer and Jitter Cleaner ICs. These are connected in a serial fashion with the first one connected to the external reference signal and the second connected to an output of the first. They have the following features:

- Two LVCMOS reference clock inputs. The secondary input is connected to the FPGA and the primary is connected to either the front panel SMB connector or an output of the first. The reference source selection is controlled by the FPGA. The reference clock can be up to 200 MHz.
- VCXO LVPECL input frequencies up to 2.2GHz. Current ESECon boards are using 156.25 MHz VCXOs.
- Output frequency is selectable by x1, /2, /3, /4, /6, /8, or /16 on each output individually.
- Device settings are SPI controllable from the FPGA.
- Outputs can be a combination of up to 10 LVCMOS or up to 5 Differential LVPECL outputs.
- PLL lock indication is an input to the FPGA.
- Efficient jitter cleaning from low PLL loop bandwidth.
- Low phase noise PLL core.

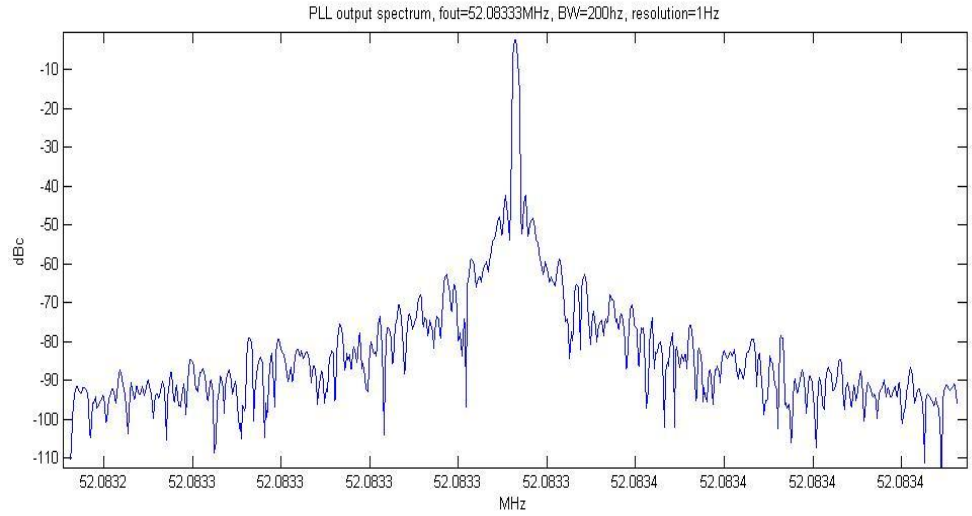
The first PLL generates LVCMOS clocks for the ADCs and the high speed serial links. It also generates duplicates of these clocks for use in the FPGA. The second PLL generates the differential LVPECL clocks for the DACs and a duplicate LVCMOS clock for use in the FPGA.

The following plots where taken with an Agilent 4395A Spectrum Analyzer. The plots were taken at the clock input on one of the ADCs with the PLL output set to divide by 3.

ADC Clock Spectrum - 10 KHz Span



ADC Clock Spectrum - 200Hz Span



ADC Information

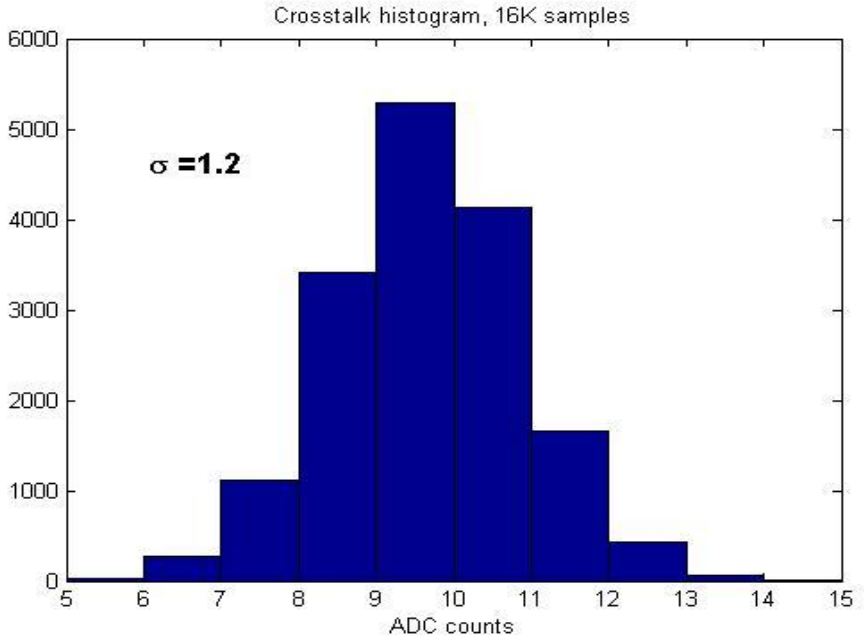
The ESECon board uses the Linear Technologies LTC2284 dual 14-bit 105Msps low power 3V ADC with the following features.

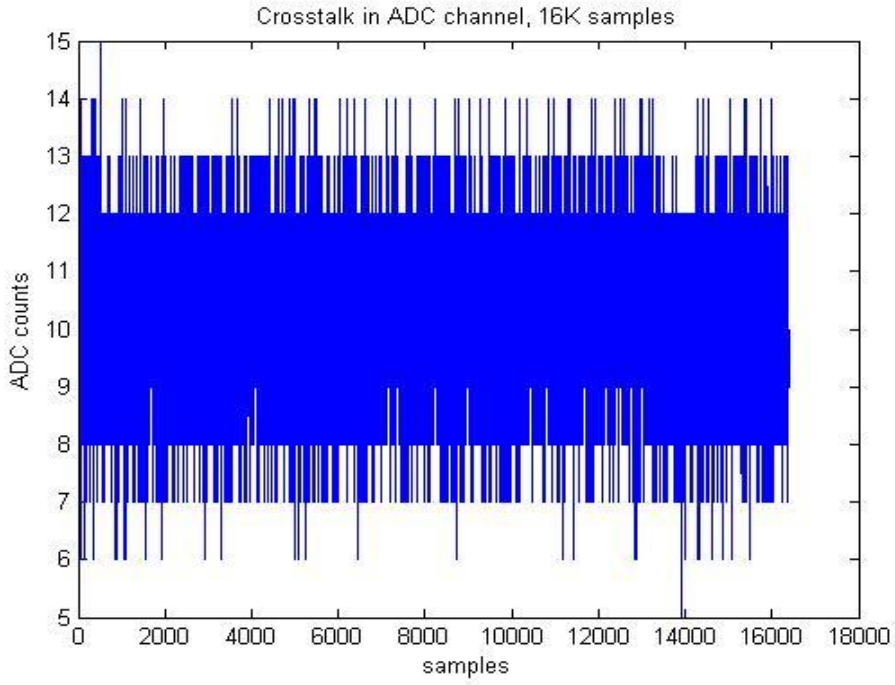
- Low power: 540mW
- 110dB channel isolation at 100MHz
- Clock duty cycle Stabilizer
- Pin compatible family of 12 and 14 bit, 10 to 125Msps ADCs

The upper eight channels are AC coupled using Tyco M/A-Com ETC1-1T RF transformers. The two lower channels can use the same input transformers or optional DC coupling using Analog Devices AD8139 amplifiers. The inputs levels are +/-1V into 50Ω on all channels.

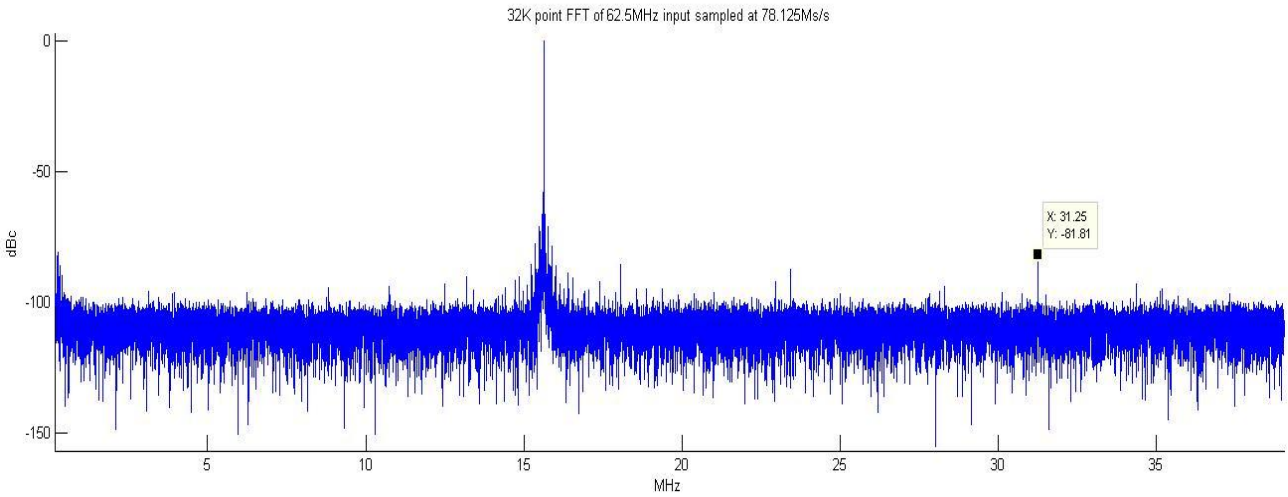
ADC Crosstalk

The following two plots show the crosstalk measured using a 50Ω terminator on one channel and a 2Vpp signal on the neighboring channel on the same device. The sampling frequency used was 78.125MHz.



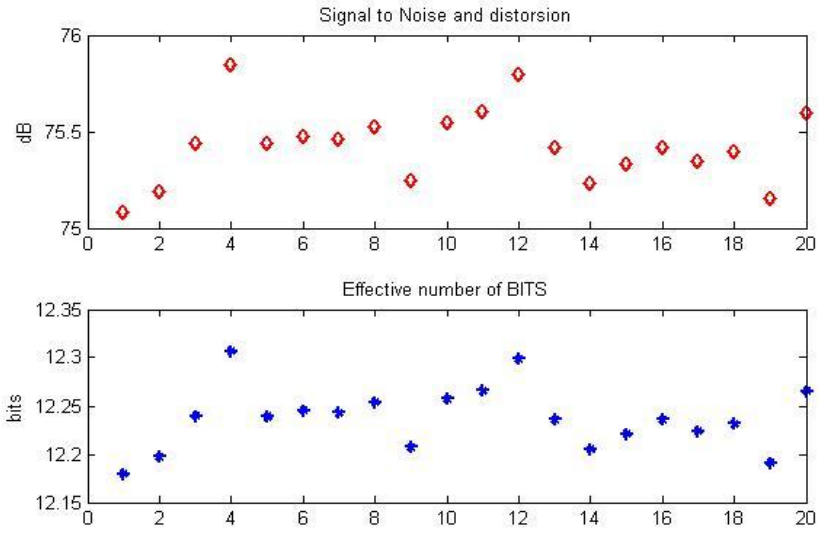


Single Tone FFT



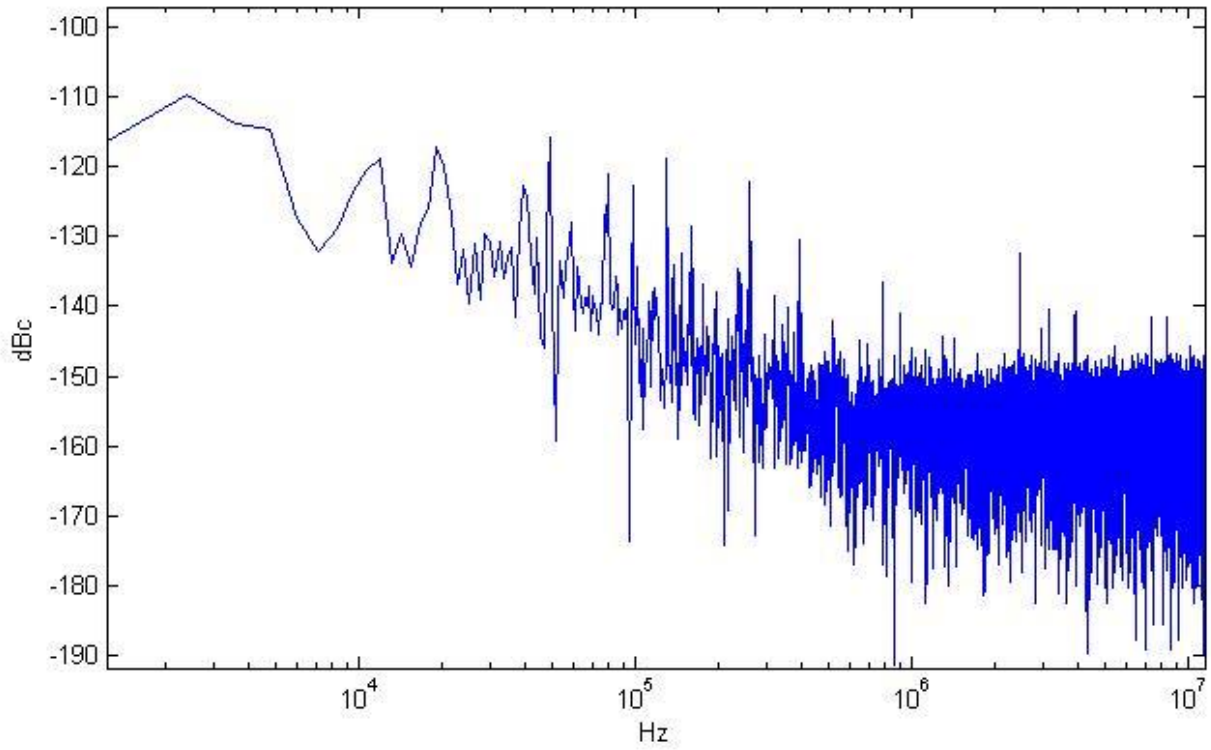
32K point FFT
SFDR = -86.1dB
SNR =75.4dB
ENOB =12.23 bits

Data sample using 4 different ADC channels.



ADC Phase Noise

ADC phase noise at zero crossing. fs=78.125MHz, fin=62.5MHz



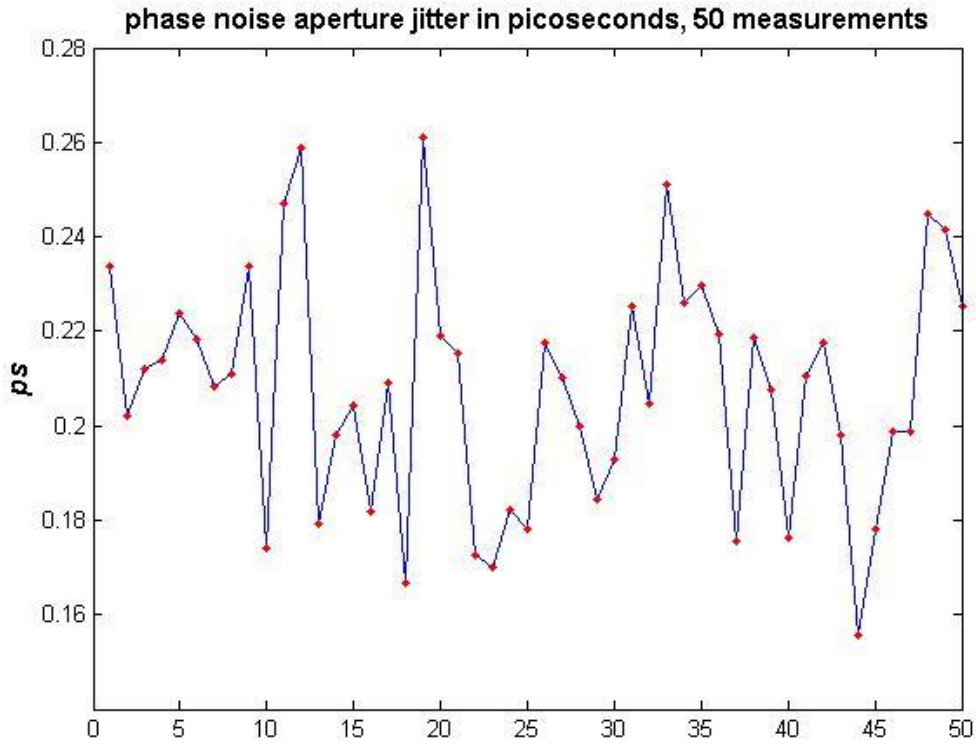
ADC Phase Jitter

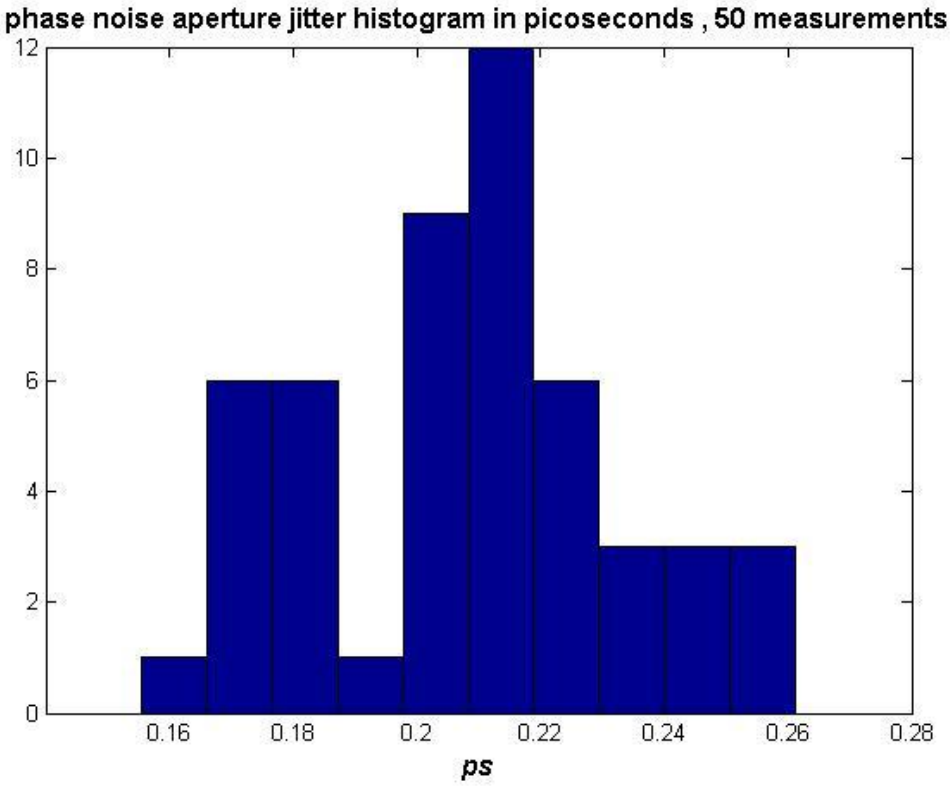
The procedure was used to create the following plots:

- Measure SNR using a low frequency input (3MHz
- Measure SNR using a high frequency input (62.5MHz)
- Calculate jitter measured by aperture time in ps

$$SNR = -20 * \log\left[\left(2\pi t_a f \right)^2 + \left(\frac{1+\varepsilon}{2^N} \right)^2 \right]^{1/2}$$

$$t_a = \frac{\sqrt{\left(10^{-SNR/20} \right)^2 - \left(\frac{1+\varepsilon}{2^N} \right)^2}}{2\pi f}$$


phase noise aperture jitter in picoseconds, 50 measurements
ps
0.28
0.26
0.24
0.22
0.2
0.18
0.16
0
5
10
15
20
25
30
35
40
45
50


phase noise aperture jitter histogram in picoseconds , 50 measurements
12
10
8
6
4
2
0
0.16
0.18
0.2
0.22
0.24
0.26
0.28
ps

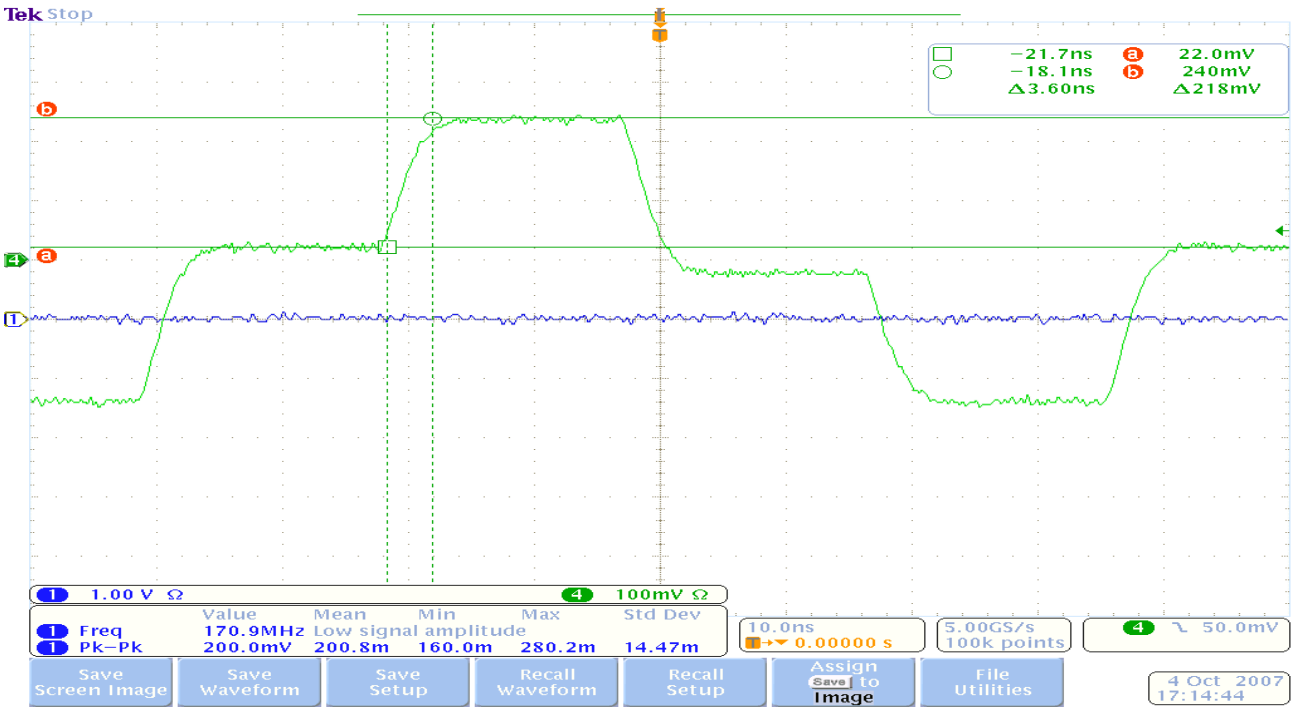
DAC Information

The ESECon board uses the Analog Devices AD9744 DAC with the following features.

- High performance member of pin-compatible TxDAC product family
- Twos complement or straight binary data format
- Power dissipation: 135 mW
- 210 MSPS update rate

The two upper channels are AC coupled using Tyco M/A-Com ETC1-1T RF transformers and the two lower channels are DC coupled using Analog Devices AD8139 Amplifiers. The output levels are +/-0.5V on the AC channels and +/-1V on the DC channels into a 50Ω load.

DAC Output - Rise Time 3ns



Front Panel I/O

The ESECon board has a 16 pin IDC connector for 8 bits of user I/O. The signals are connected to the Xilinx FPGA through TI SN74LVTH241 transceivers. The direction is controlled by the FPGA and is in two groups of four. The input buffers support both 5V and 3.3V TTL signal levels. The output buffers are LVTTL and can drive 32 mA and sink 64 mA of current.

High Speed Serial Links

The two high speed serial links are controlled by the Xilinx FPGA and utilize Texas Instruments TLK2501 1.5 to 2.5 GBPS Transceivers. The TLK2501 provides up to 2 GBPS of data bandwidth. The TLK2501 is both pin-for-pin compatible with and functionally identical to the TLK1501, a 0.6 to 1.5 GBPS transceiver, and the TLK3101, a 2.5 to 3.125 GBPS transceiver, providing a wide range of performance solutions.

Each TLK2501 connects to a Small Form-factor Pluggable (SFP) transceiver connector and card cage through the front panel. This industry standard allows for either optical or copper links to be used via plug in transceiver modules.

Each SFP has front panel indicator LEDs for loss of signal (LOS) and transmitter fault (TXFAULT).

Daughter Card Connector

There is a Tyco/AMP MICTOR 114 signal and 15 ground pin daughter card connector for adding custom CPU, DSP, or logic functions. The connector provides the following connections.

- 86 I/O signals to the Xilinx FPGA
- 28 Power pins for 5V, 3.3V, 2.5V, 1.8V, and 1.2V
- 15 ground connections

User Front Panel LEDs

There are 8 Xilinix firmware defined LEDs and 4 Altera firmware defined LEDs on the front panel.

SYSTEM SOFTWARE AND FIRMWARE

SYSTEM SOFTWARE AND FIRMWARE

Software

Firmware

The original firmware has been carried over from the DESY designed SIMCON3.1 module. This firmware was created using hierarchical VHDL and custom libraries. We used this firmware with its hierarchical structure as a base platform to build upon and then add our own custom algorithms to the design.

The controller functions that are implemented in VHDL include:

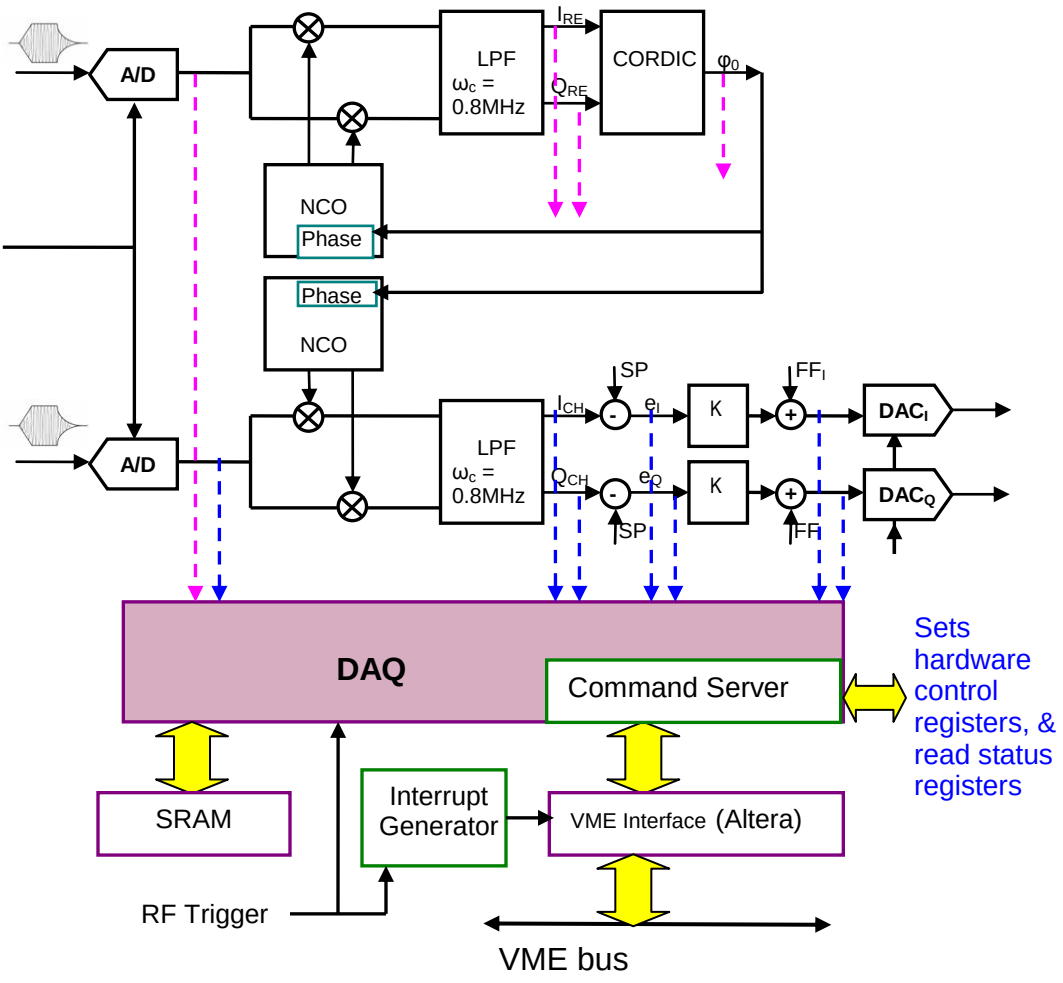
- VME interface and on-board internal interface
- Hardware control and status registers
- Data acquisition interface to onboard memory (SRAM)
- DAQ and control timing

The ESE LLRF Controller implements complex control algorithms. These algorithms contain various digital signal processing (DSP) functions such as numeric controlled oscillators (NCO), digital up-down conversion, CIC/FIR filters, multipliers, and accumulators. These control algorithms will undergo numerous cycles of development, verification, refinement, and testing. In an effort to make this iterative process more efficient, the firmware is currently being developed using a graphical environment tool suite from both Mathworks and Xilinx. The tool suite includes Matlab, Simulink, and System Generator for DSP. The current ESE Controller firmware includes various signal processing algorithms and control functions that make use of elements called Intellectual Property (IP) blocks found in the Xilinx System Generator for DSP library. These IP blocks implement commonly used DSP functions and are optimized to take advantage of the Virtex-4 FPGA resources efficiently. Using these tools allow us to both build complex control algorithms and then model these algorithms in the Simulink graphical environment. These models are then added as components to the hierarchical VHDL.

This is a list of the functions in the ESE Controller that have been implemented using the Matlab-Simulink-System Generator graphical environment:

- Reference channel with automatic phase tracking using a Cordic algorithm
- Digital down converter (DDS) with tunable frequency
- 2-stage CIC-FIR digital low pass filter
- Proportional-integral (PI) gain control
- Digital up-conversion to IF with offset and gain control

The figure below illustrates some of the key elements in the firmware.



4 INTERFACE SPECIFICATIONS

4.1 ESE Controller Register Map

This is the ESE Controller's current register map.

4.1.1 Signal Descriptions

Module Number (0x000): This is the module identification number. It is hard coded into the firmware and the value is currently 0x1.

ASCII Name 1 (0x004): A 32-bit register that contains the name of the controller in ASCII format. Address 0x004 contains "ESE".

ASCII Name 2 (0x008): A 32-bit register that contains the name of the controller in ASCII format. Address 0x008 contains "CON1".

Firmware Version (0X00C): A 32-bit register that contains the name of the firmware version in the controller in ASCII format. Current versions are: CC1, CC2, NML, RFG, and RTS.

Firmware Date (0X010): This is currently the firmware version tracking register. The 32-bit register format has been defined as 4 bytes that contain the year (MSB), month, day, and hour (LSB) in which the firmware version was compiled.

User Register (0x014): This is a 32-bit register that is read/write by the user.

Interface API (0x018): The software uses the value in this register to determine the appropriate version of the register map.

Local Resetn (0x01C, bit 0): This is the active low reset signal to initialize various logic on the controller board. On power-up the reset is zero (active). You must set this bit to a one for the board to operate.

Select External Trigger (0x020, bit 0): Default value is zero. When this bit is zero, the module uses an internally generated one second trigger and one microsecond strobe for control and acquisition timing. When set to a one, you must provide the trigger as a TTL level signal to the front panel IDC connector pin 1.

External Trigger Failed (0x024, bit 0): This is a status register. If register bit 0 is zero, the controller is detecting a 1Hz or higher rate external trigger pulse from the front panel IDC connector pin 1. If register bit 0 is one, the board is not detecting this trigger pulse.

Interrupt Enable (0x028, bit 0): When this bit is zero, VME interrupt is disabled. When set to one, the module will generate a VME interrupt level 7 at the trigger rate immediately after the control cycle completes.

Feedforward Enable (0x02C, bit 0): Default value is zero. When this bit is zero, feedforward is disabled. When set to one, feedforward is enabled.

Feedback Enable (0x030, bit 0): Default value is zero. When this bit is zero, feedback is disabled. When set to one, feedback is enabled.

Select External Reference (0x034, bit 0): The default value is zero. When this bit is zero, the onboard PLL will be free running at 46.2MHz. When set to one, onboard PLL will lock to the externally supplied clock. This clock is a 3 volt TTL signal supplied to the front panel SMB connector labeled RCK. This version of the firmware expects the frequency to be 50MHz.

External Reference Failed (0x038, bit 0): When set to one, the onboard PLL is not locked to the externally supplied clock.

Program PLL Externally (0x03C, bit 0): Default value is zero. When this bit is zero, the firmware configures the two onboard PLLs. When set to one, the PLLs can be programmed through the front panel connector with the manufacturer supplied GUI tool.

ADC PLL Enable (0x040, bit 0): Default value is zero. When this bit is zero, the firmware uses hard coded values to configure the ADC PLL. When set to one, the firmware uses the values in the two registers (WORD_ADC_VXO_REF and WORD_ADC_Y4_0_FB_CP) to configure the ADC PLL.

DAC PLL Enable (0x044, bit 0): Default value is zero. When this bit is zero, the firmware uses hard coded values to configure the DAC PLL. When set to one, the firmware uses the values in the two registers (WORD_DAC_VXO_REF and WORD_DAC_Y4_0_FB_CP) to configure the DAC PLL.

Stop Acquire (0x048, bit 0): The default value is zero. When this bit is zero, the data acquisition and control functions run at the trigger rate. When set to one, the data acquisition and control functions are stopped to allow memory readout.

Select Table (0x04C, bit 0): The default value is zero. When this bit is zero, feedforward and setpoint values from table 1 are used in the control cycle. When set to one, feedforward and setpoint values from table 2 are used in the control cycle.

Select Address Pointer (0x050, bit 0): The default value is zero. When zero, use value in Address Pointer 1. When set to one, use value in Address Pointer 2.

Address Pointer 1 (0x054, bits 31 - 0): The default value is 0x0000000. Stores acquisition data starting at this offset.

Address Pointer 2 (0x058, bits 31 - 0): The default value is 0x0100000. Stores acquisition data starting at this offset.

Channel Gain Overflow (0x05C, bit 0): When set to one, the signal into ADC channel 2 has exceeded the dynamic range of the internal data path. Reduce the Channel 2 Gain value.

Interrupt Level (0x060, bits 2 - 0): The default value is 0x7. Used to set the VME interrupt level 1-7.

I Feed Forward Scaler (0x064, bits 17 - 0): Multiplier used to scale and rotate the (I) feed forward table vector.

Q Feed Forward Scaler (0x068, bits 17 - 0): Multiplier used to scale and rotate the (Q) feedforward table vector.

I Set Point Scaler (0x06C, bits 17 - 0): Multiplier used to scale and rotate the (I) set point table vector.

Q Set Point Scaler (0x070, bits 17 - 0): Multiplier used to scale and rotate the (Q) set point table vector.

DAC 1 Offset (0x074, bits 17 - 0): Offset 1 is not used in this version of the firmware.

DAC 2 Offset (0x078, bits 17 - 0): Offset 2 is not used in this version of the firmware.

DAC 3 Offset (0x07C, bits 17 - 0): Offset 3 controls the DC +/- offset from zero for DAC output 3.

DAC 4 Offset (0x080, bits 17 - 0): Offset 4 controls the DC +/- offset from zero for DAC output 4.

IF Frequency (0x084, bits 31 - 0): Default value is 0x4808dda5. Numeric controlled oscillator output frequency. This register is used to match the Intermediate Frequency (IF) applied to ADC1. The equation to compute the value is: register value = Fout * 2^32/Fin.

Integral Gain (0x088, bits 19 - 0): This register value is the integral gain that is applied in the PI controller section when feedback is enabled. The format is 20 - bits integer. Register bits 31-20 are unused.

Proportional Gain (0x08C, bits 19 - 0): This register value is the proportional gain that is applied in the PI controller section when feedback is enabled. The format is 12-bits integer and 8-bits fractional. The power up default value is 0x00100, which is a gain of one. Register bits 31-20 are unused.

Feedforward Delay (0x090, bits 15 - 0): Default value is zero. A 16-bit counter clocked at 46.2MHz. Used to delay the assertion of the feedforward table values in the controller cycle after receiving the trigger pulse.

Setpoint Delay (0x094, bits 15 - 0): Default value is zero. A 16-bit counter clocked at 46.2MHz. Used to delay the assertion of the setpoint table values in the controller cycle after receiving the trigger pulse.

Cycle Length (0x098, bits 15 - 0): This counter sets the length of time that the controller stores the data acquired during the cycle. Each count in this register corresponds to 1 microsecond. The hard-coded value is 0x3400.

Control Length (0x09C, bits 15 - 0): This counter sets the length of time that the PI control actively regulates the cavity during the cycle. Each count in this register corresponds to 1 microsecond. The hard-coded value is 0x3400.

ADC VXO Reference (0x0A0, bits 31 - 0): This register can be used to set various parameters of the ADC PLL. This register was used for board debugging. On power-up, PLL initialization is handled by using values hard-coded in the firmware.

ADC Y4-0 FB CP (0x0A4, bits 31 - 0): This register can be used to set various parameters of the ADC PLL. This register was used for board debugging. On power-up, PLL initialization is handled by using values hard-coded in the firmware.

DAC VXO Reference (0x0A8, bits 31 - 0): This register can be used to set various parameters of the DAC PLL. This register was used for board debugging. On power-up, PLL initialization is handled by using values hard-coded in the firmware.

DAC Y4-0 FB CP (0x0AC, bits 31 - 0): This register can be used to set various parameters of the DAC PLL. This register was used for board debugging. On power-up, PLL initialization is handled by using values hard-coded in the firmware.

DUC Phase (0x0B0, bits 31 - 0): This register controls the digital up-converter (DUC) phase shift relative to the phase on the incoming reference signal. The control signal is up-converted to IF and drives DAC1 and DAC2.

I DUC Offset (0x0B4, bits 15 - 0): This register controls the digital up-converter (DUC) phase offset relative to the phase on the incoming reference signal. The control signal is up-converted to IF and drives DAC1.

Q DUC Offset (0x0B8, bits 15 - 0): This register controls the digital up-converter (DUC) phase offset relative to the phase on the incoming reference signal. The control signal is up-converted to IF and drives DAC2.

I DUC Gain (0x0BC, bits 15 - 0): This register controls the amount of gain applied to the output signal. The control signal is up-converted to IF and drives DAC1. The format is 8-bits integer and 8-bits fractional. The power up default value is 0x0100, which is a gain of one. Register bits 31-16 are unused.

Q DUC Gain (0x0C0, bits 15 - 0): This register controls the amount of gain applied to the output signal. The control signal is up-converted to IF and drives DAC2. The format is 8-bits integer and 8-bits fractional. The power up default value is 0x0100, which is a gain of one. Register bits 31-16 are unused.

Channel 1 Gain (0x0C4, bits 15 - 0): Not used in this version of the firmware.

Channel 1 Phase (0x0C8, bits 31 - 0): Channel 1 is the input IF phase reference channel.

Channel 2 Gain (0x0CC, bits 15 - 0): This register value is the gain that is applied to the signal into ADC 2. The format is 8-bits integer and 8-bits fractional. The power up default value is 0x0100, which is a gain of one. Register bits 31-16 are unused.

Channel 2 Phase (0x0D0, bits 31 - 0): This register value is the phase offset relative to the IF phase reference into Channel 1.

Channel 3 Gain (0x0D4, bits 15 - 0): This register value is the gain that is applied to the signal into ADC 3. The format is 8-bits integer and 8-bits fractional. The power up default value is 0x0100, which is a gain of one. Register bits 31-16 are unused.

Channel 3 Phase (0x0D8, bits 31 - 0): This register value is the phase offset relative to the IF phase reference into Channel 1.

Channel 4 Gain (0x0DC, bits 15 - 0): This register value is the gain that is applied to the signal into ADC 4. The format is 8-bits integer and 8-bits fractional. The power up default value is 0x0100, which is a gain of one. Register bits 31-16 are unused.

Channel 4 Phase (0x0E0, bits 31 - 0): This register value is the phase offset relative to the IF phase reference into Channel 1.

Channel (5-10) Gain (0x0XX, bits 15 - 0): Not used in this version of the firmware.

Channel (5-10) Phase (0x0XX, bits 31 - 0): Not used in this version of the firmware.

Event Count (0x114, bits 7 - 0): 8-bit counter accumulates the number of triggered events that occurred and rolls over to zero.

Continuous Wave Node (0x118, bit 0): The default value is zero. When set to one, the controller DAC output will hold the last value in the feedforward table.

Path Delay (0x11C, bits 7 - 0): Default value is zero. An 8-bit counter clocked at 46.2MHz. Used to increase the delay in the feedback path.

I Feedforward Table 1 (0x10000, bits 17 - 0): I values of feedforward table 1.

Q Feedforward Table 1 (0x14000, bits 17 - 0): Q values of feedforward table 1.

I Setpoint Table 1 (0x18000, bits 17 - 0): I values of setpoint table 1.

Q Setpoint Table 1 (0x1C000, bit bits 17 - 0): Q values of setpoint table 1.

I Feedforward Table 2 (0x20000, bits 17 - 0): I values of feedforward table 2.

Q Feedforward Table 2 (0x24000, bits 17 - 0): Q values of feedforward table 2.

I Setpoint Table 2 (0x28000, bits 17 - 0): I values of setpoint table 2.

Q Setpoint Table 2 (0x2C000, bit bits 17 - 0): Q values of setpoint table 2.

SRAM Start (0x100000, bits 17 - 0): The starting address of onboard SRAM where the controller stores data acquired during the control cycle.